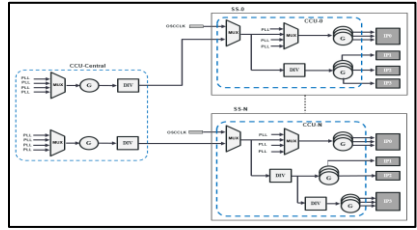
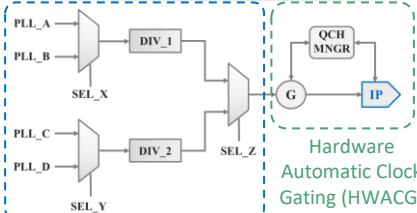


INTRODUCTION

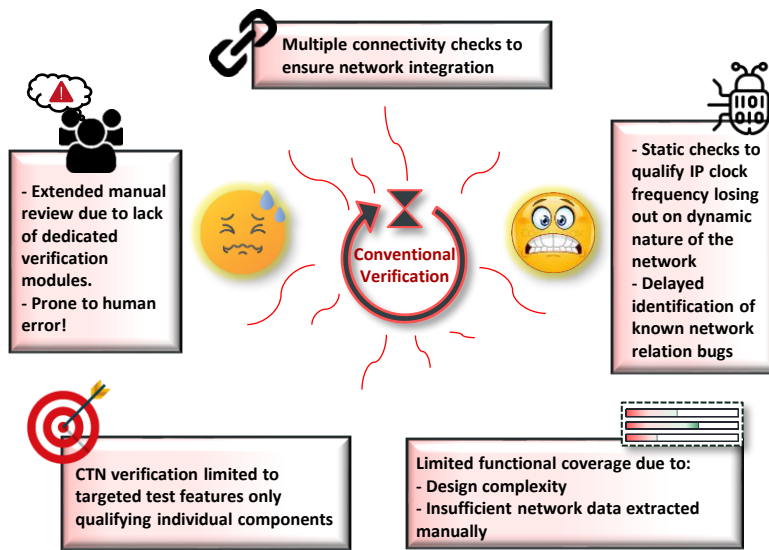


Clock Tree Network

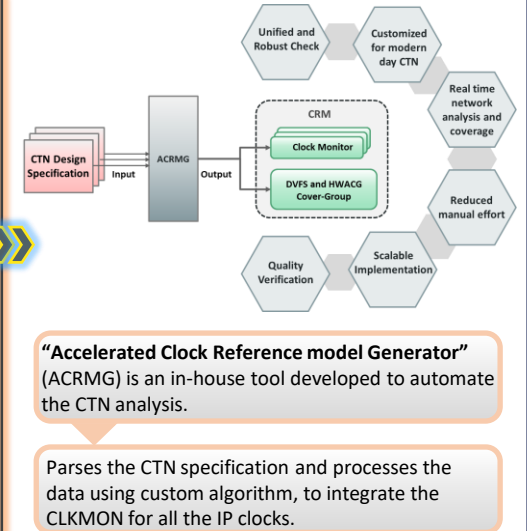


Dynamic Voltage Frequency Scaling (DVFS)

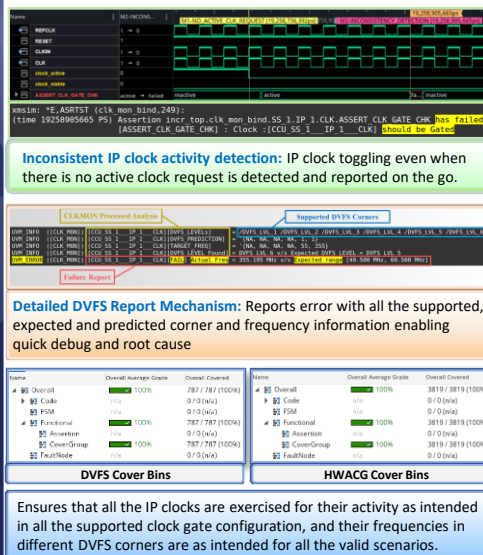
PROBLEM STATEMENT



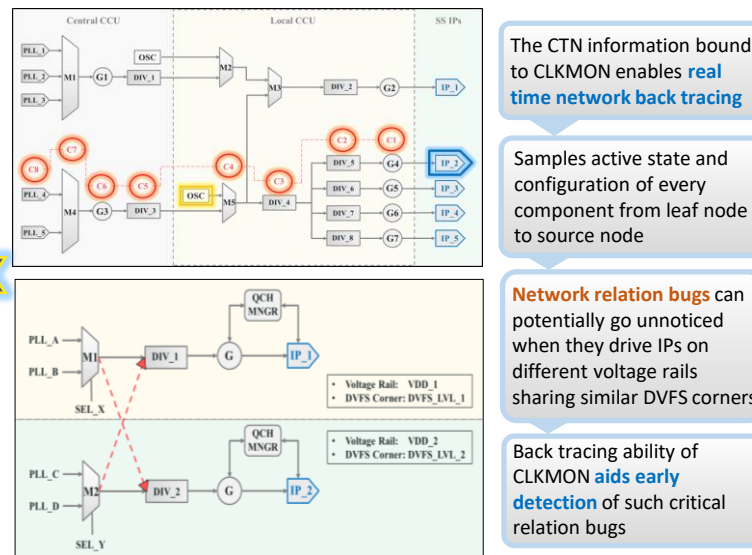
PROPOSED SOLUTION



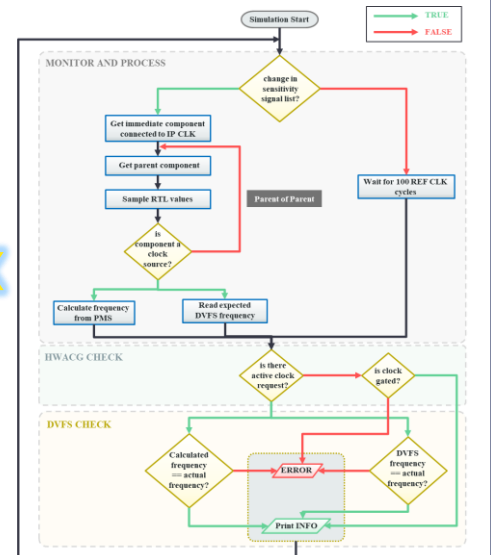
RESULTS



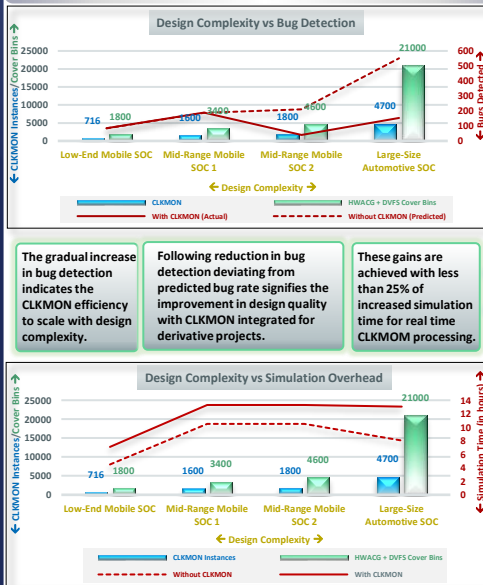
DEPLOYMENT



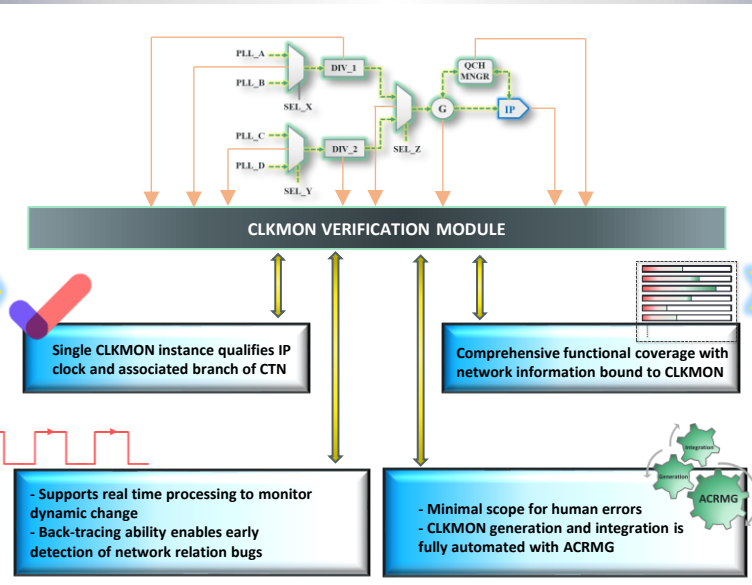
OPERATIONAL FLOW



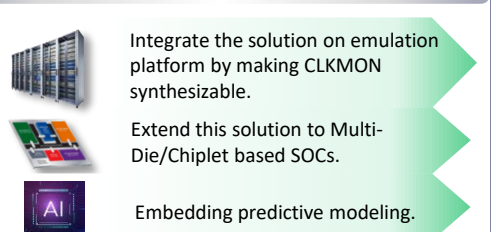
RESULTS



OUTCOME



FUTURE SCOPE



REFERENCES

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- Tejas Dipakkumar Dalal, Giridhar S, Jeevan Nataraju, Garima Srivastava, "Quality Driven Analysis of Clock Tree Network using Accelerated Clock Reference Model Generator", in DVCon Japan, Aug. 2024, in press.
- AMBA Low Power Interface Specification, ARM Standard IHI 0068C (ID091216)